FIG. 1

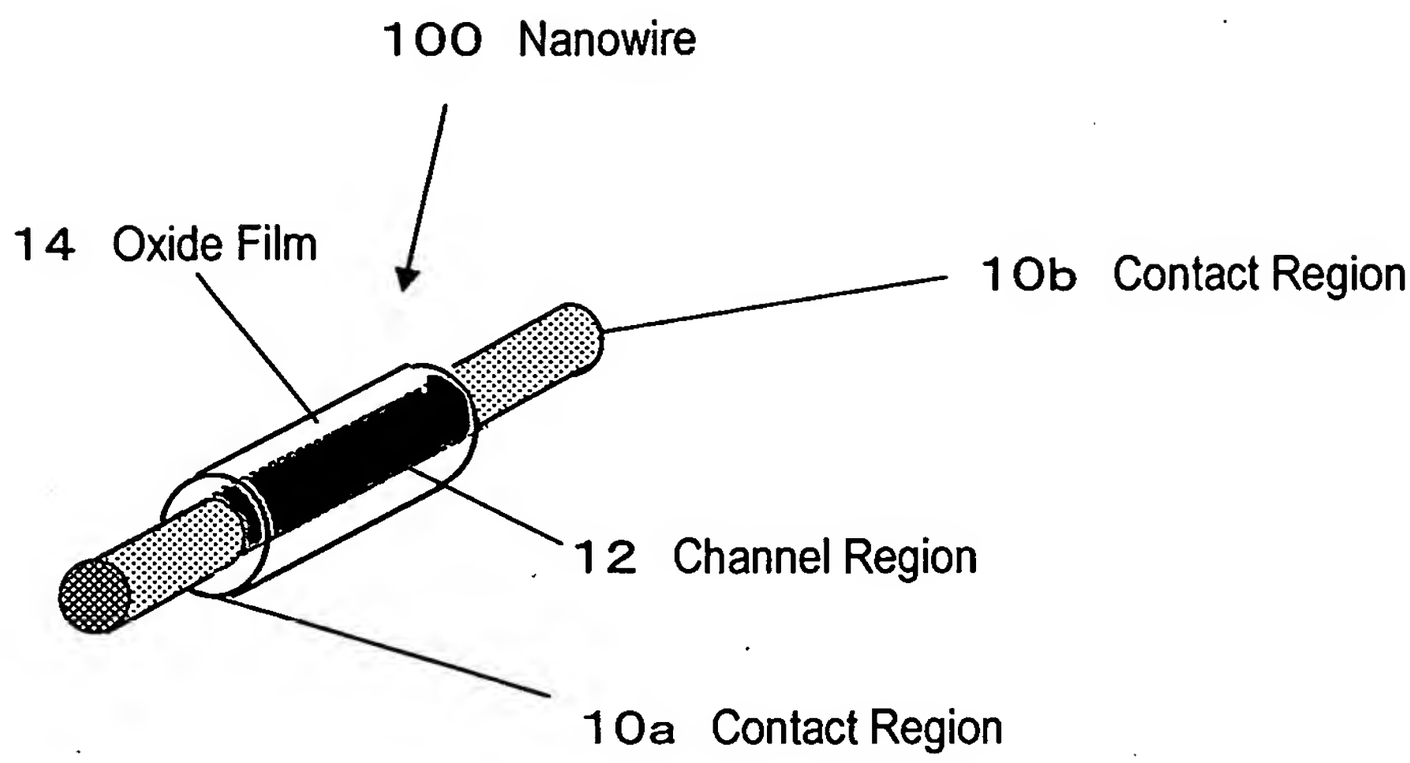
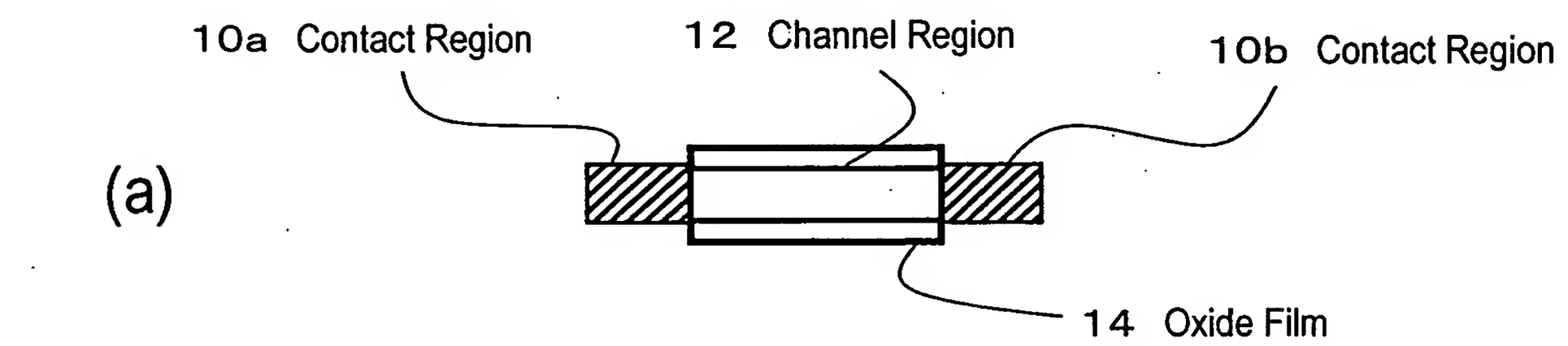

100 Nanowire
14 Oxide Film
10b Contact Region
12 Channel Region
10a Contact Region

FIG. 2


(a)
10a Contact Region
12 Channel Region
10b Contact Region
14 Oxide Film

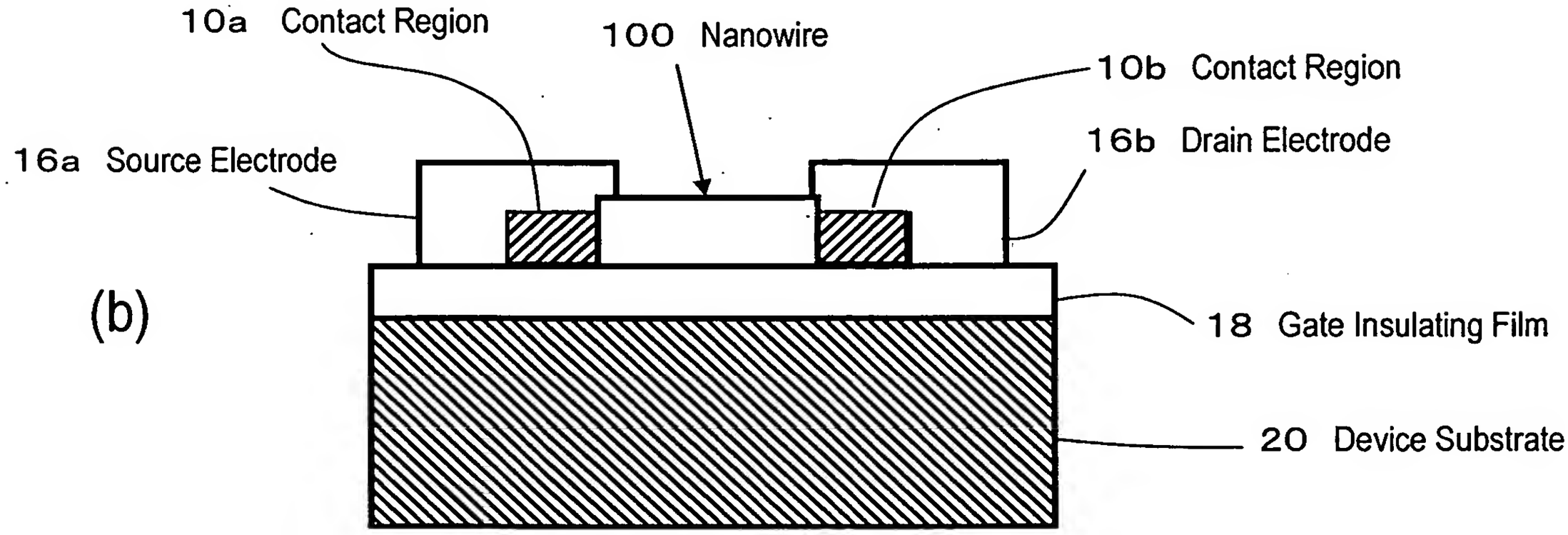
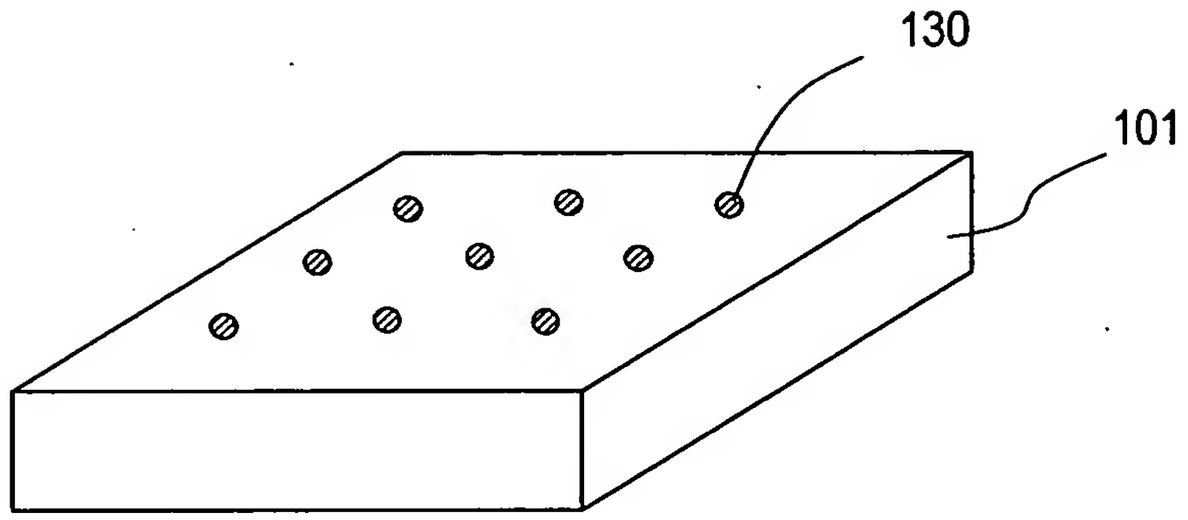
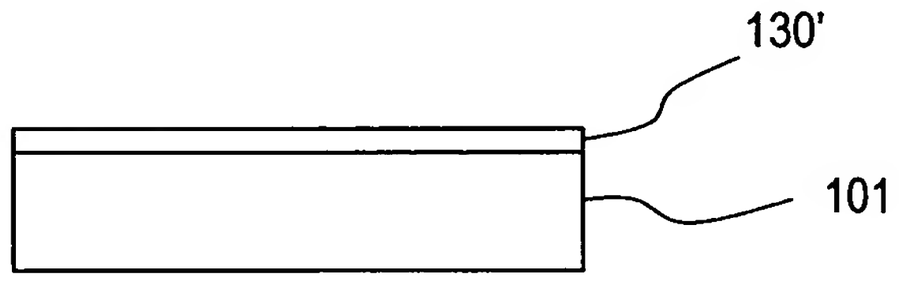

(b)
10a Contact Region
100 Nanowire
10b Contact Region
16a Source Electrode
16b Drain Electrode
18 Gate Insulating Film
20 Device Substrate

FIG. 3

(a)




(b)




(c)

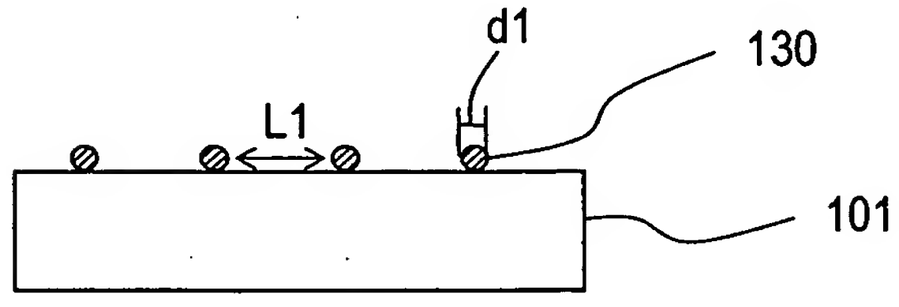
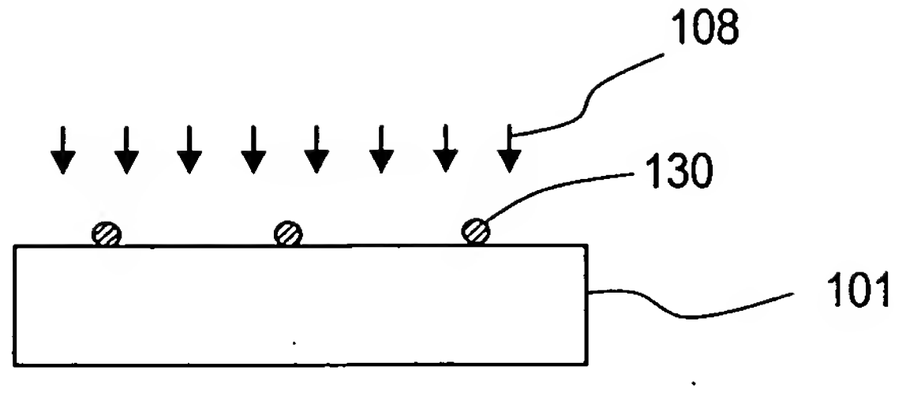
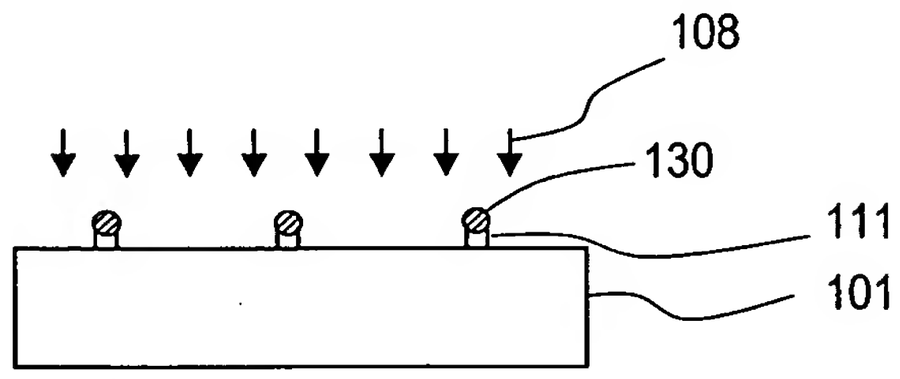


FIG. 4

(a)




(b)




(c)

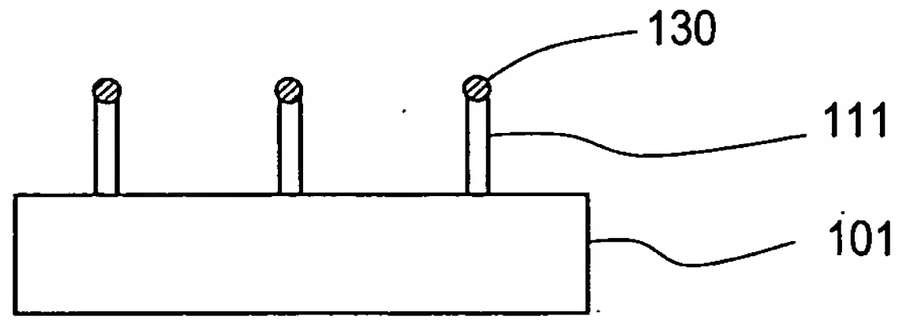
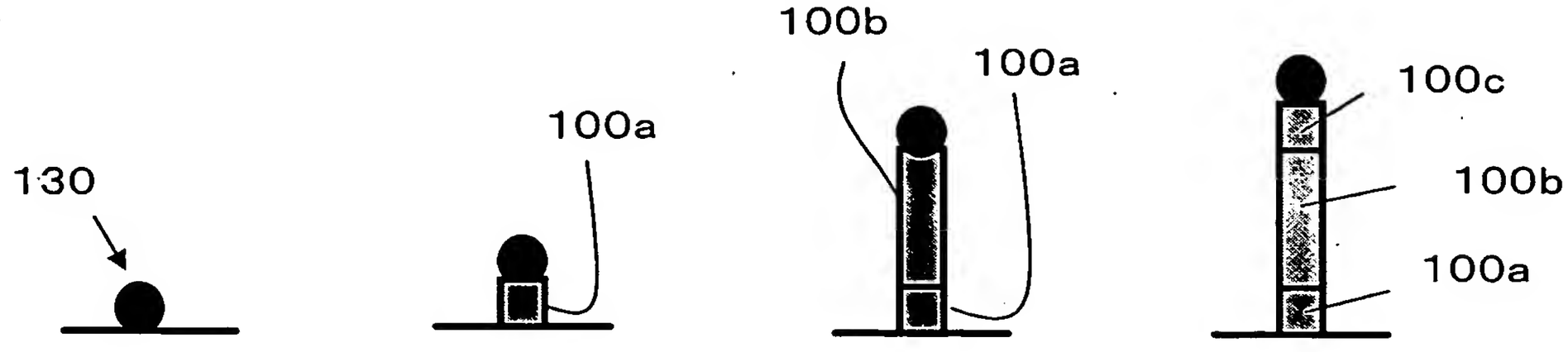


FIG. 5




(a) (b) (c) (d)

(e) (f) (g)

FIG. 6

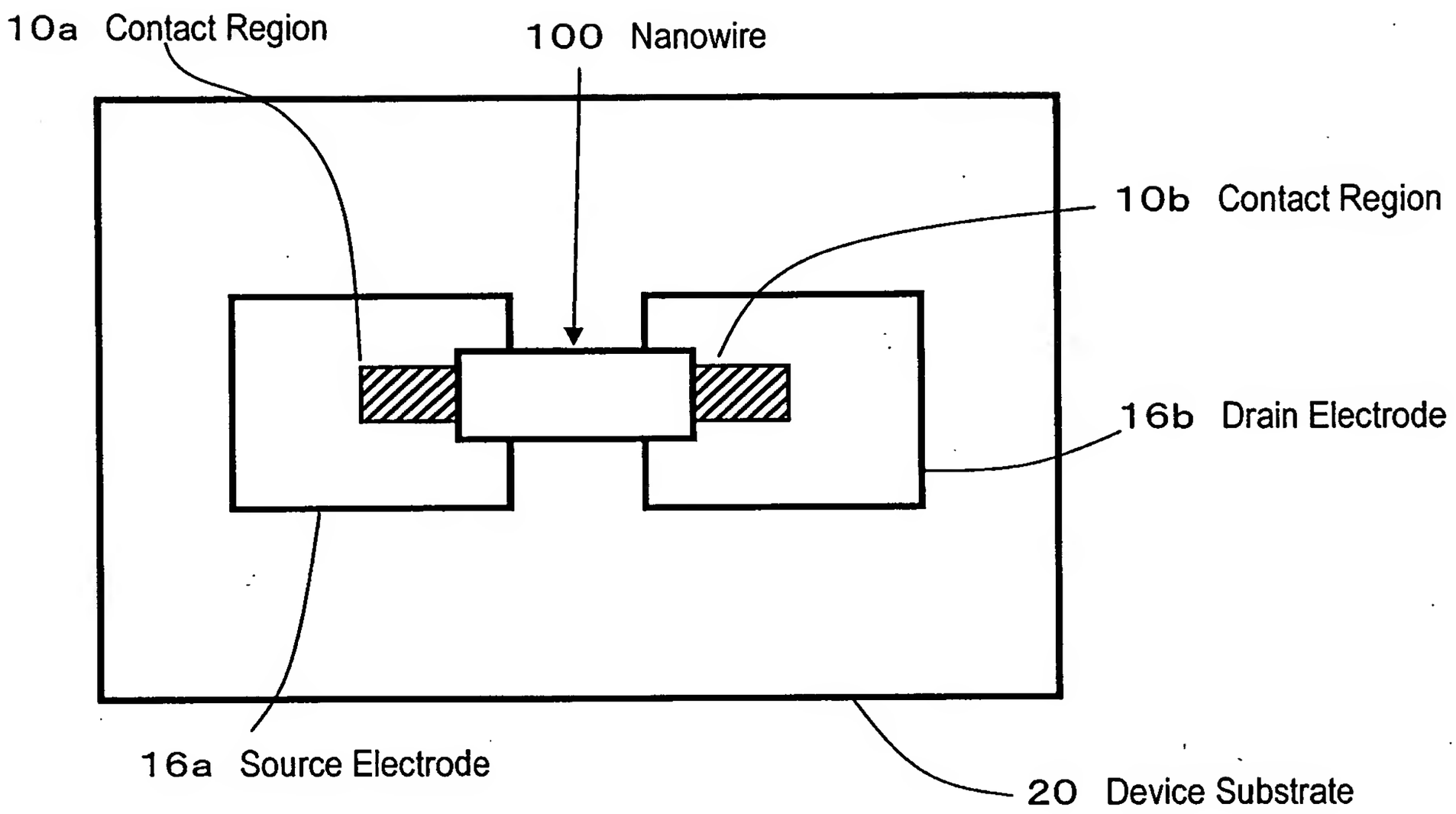

10a Contact Region
100 Nanowire
10b Contact Region
16b Drain Electrode
16a Source Electrode
20 Device Substrate

FIG. 7

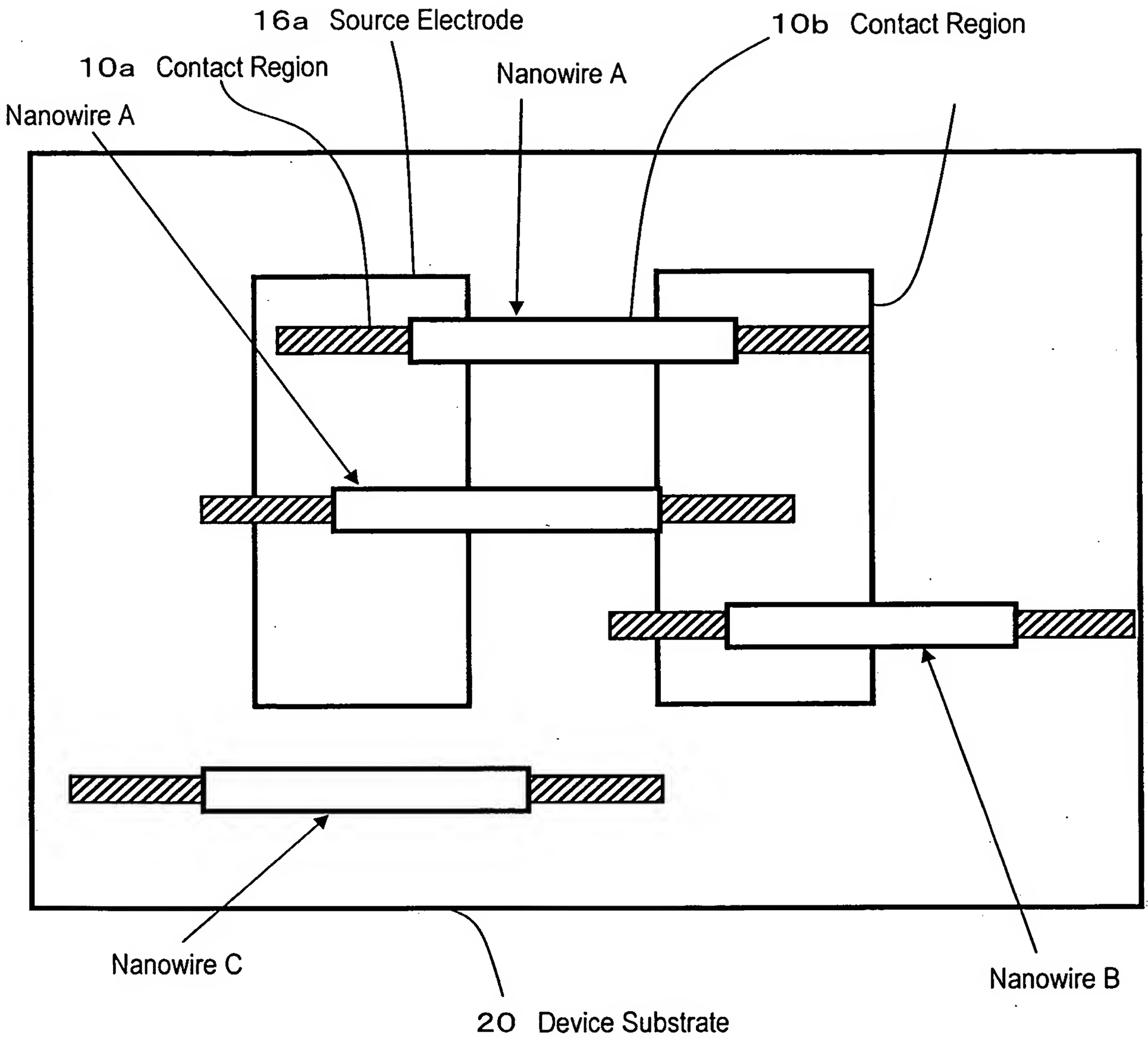

16a Source Electrode
10a Contact Region
Nanowire A
Nanowire A
10b Contact Region
Nanowire C
20 Device Substrate
Nanowire B

FIG. 8

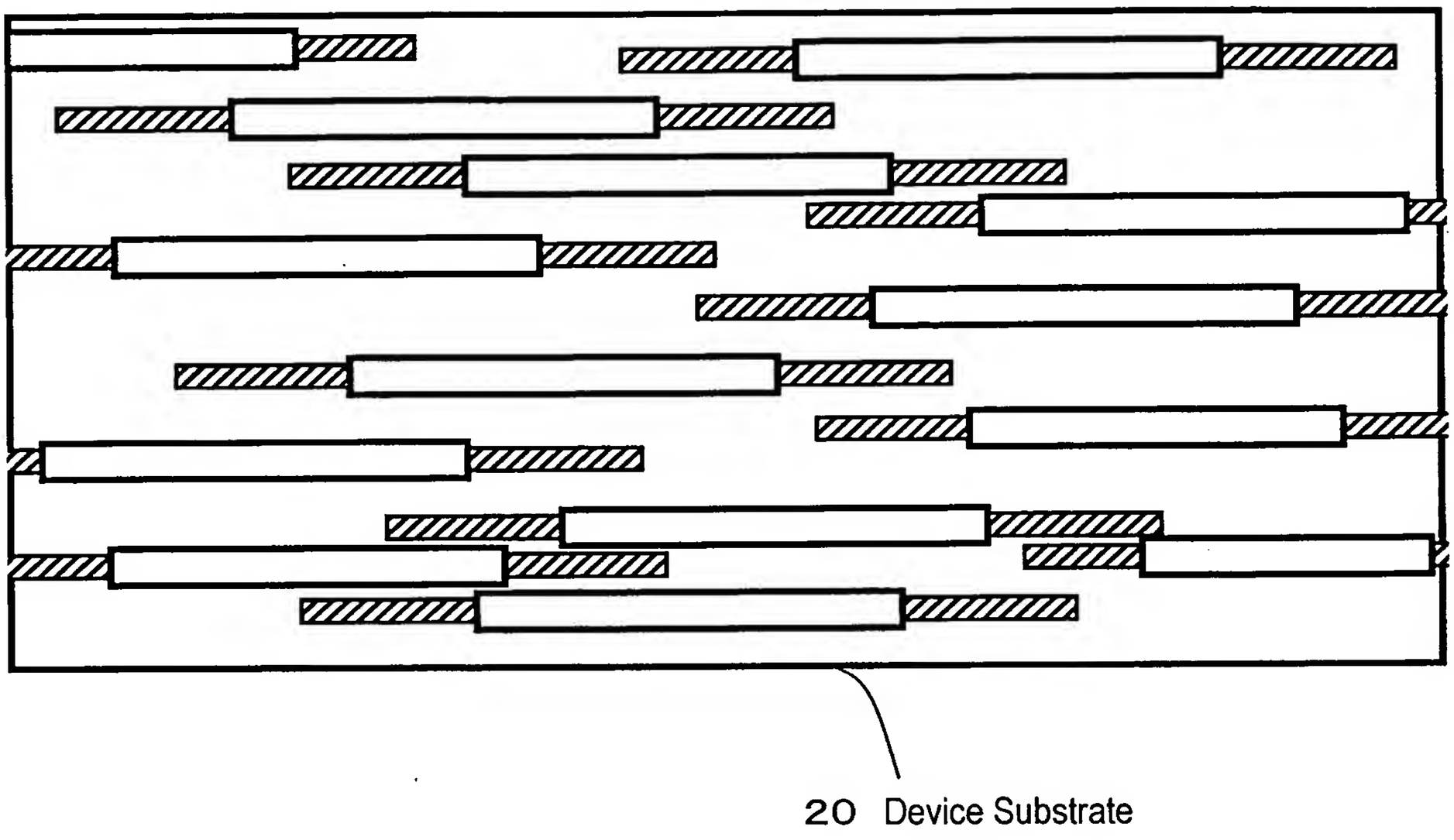
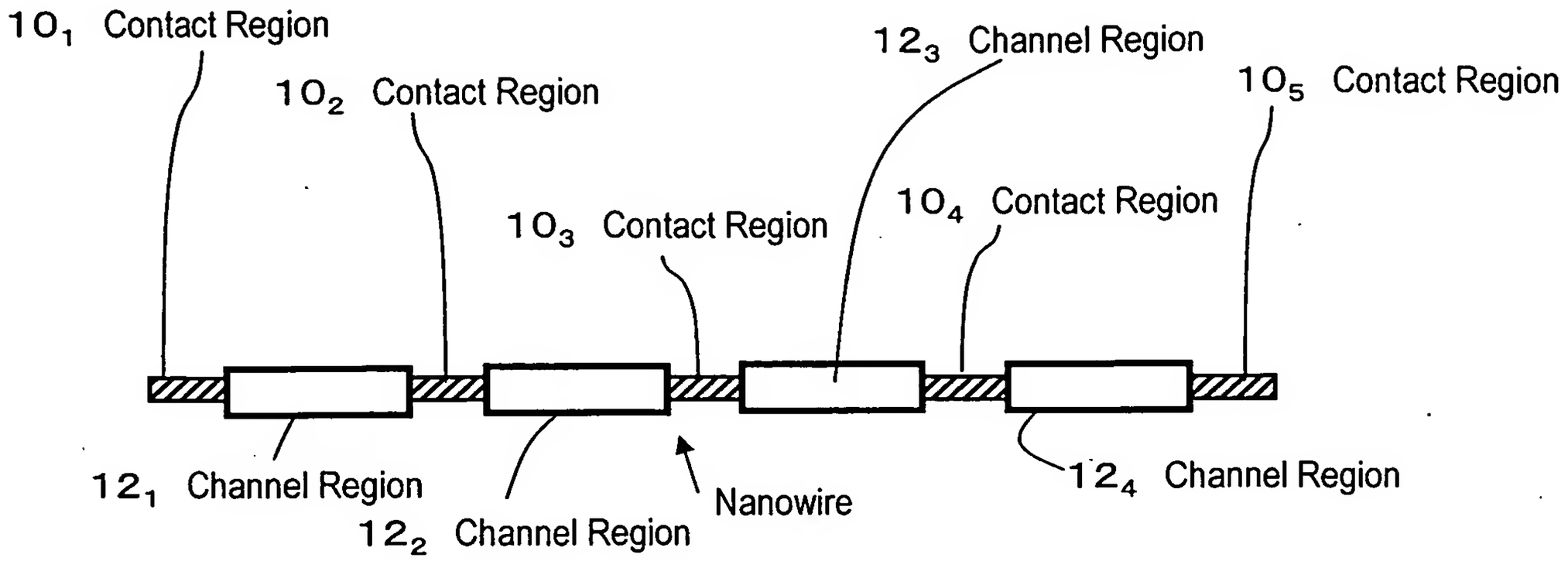


FIG. 9

(a)


10₁ Contact Region
10₂ Contact Region
12₃ Channel Region
10₅ Contact Region
10₃ Contact Region
10₄ Contact Region
12₁ Channel Region
12₂ Channel Region
Nanowire
12₄ Channel Region

(b)

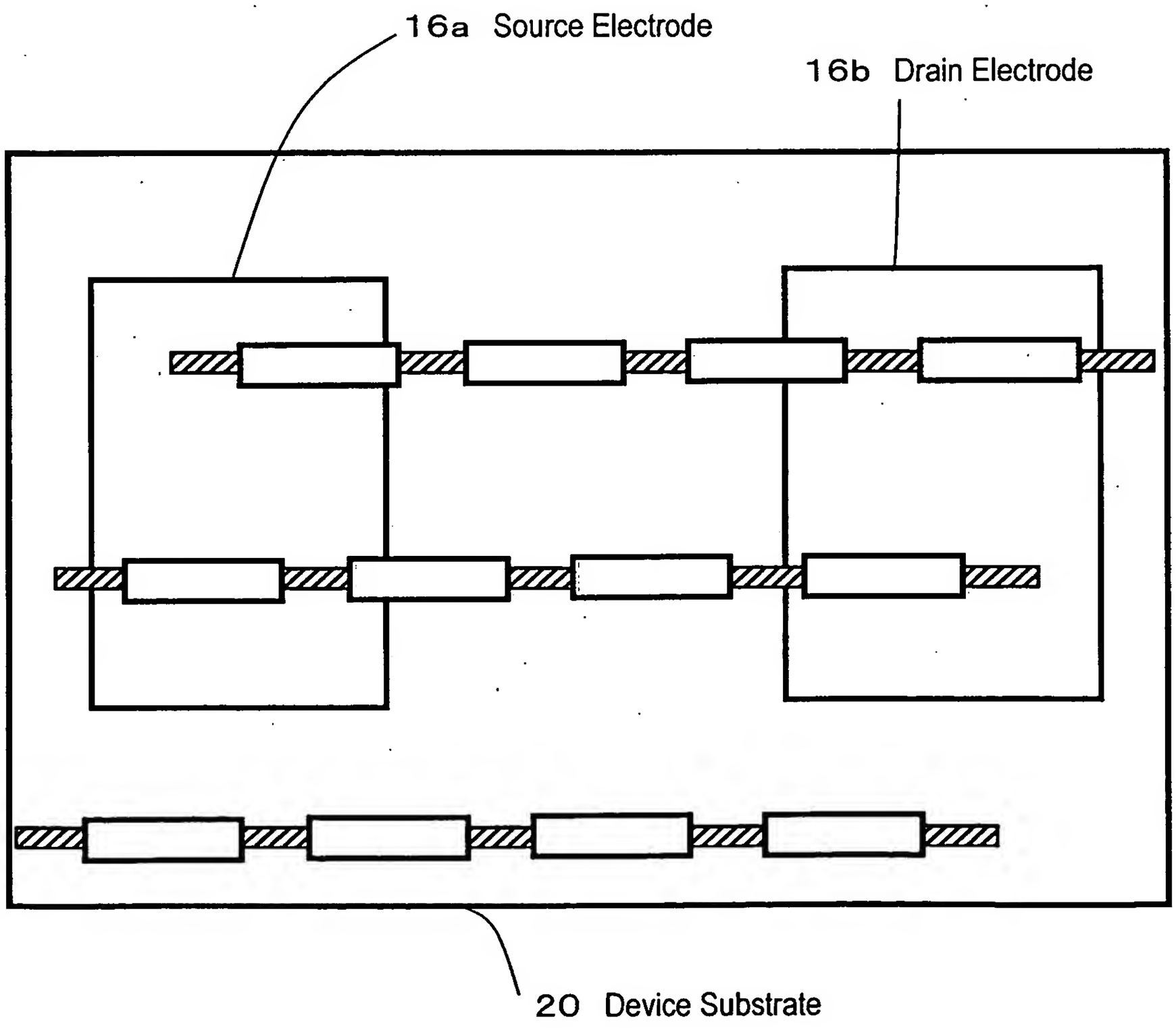

16a Source Electrode
16b Drain Electrode
20 Device Substrate

FIG. 10

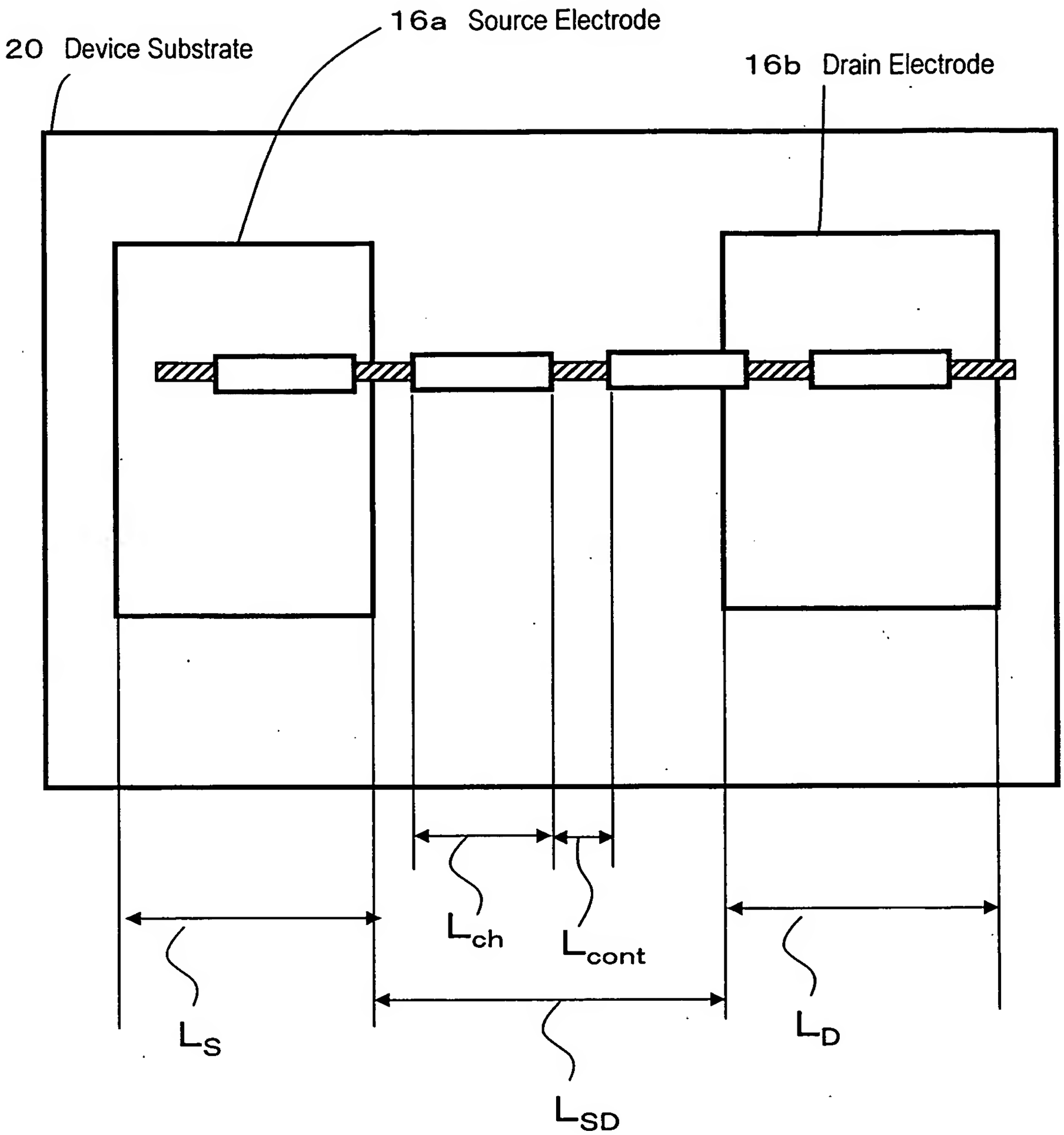

20 Device Substrate
16a Source Electrode
16b Drain Electrode
$L_{ch}$
$L_{cont}$
$L_S$
$L_D$
$L_{SD}$

FIG. 11

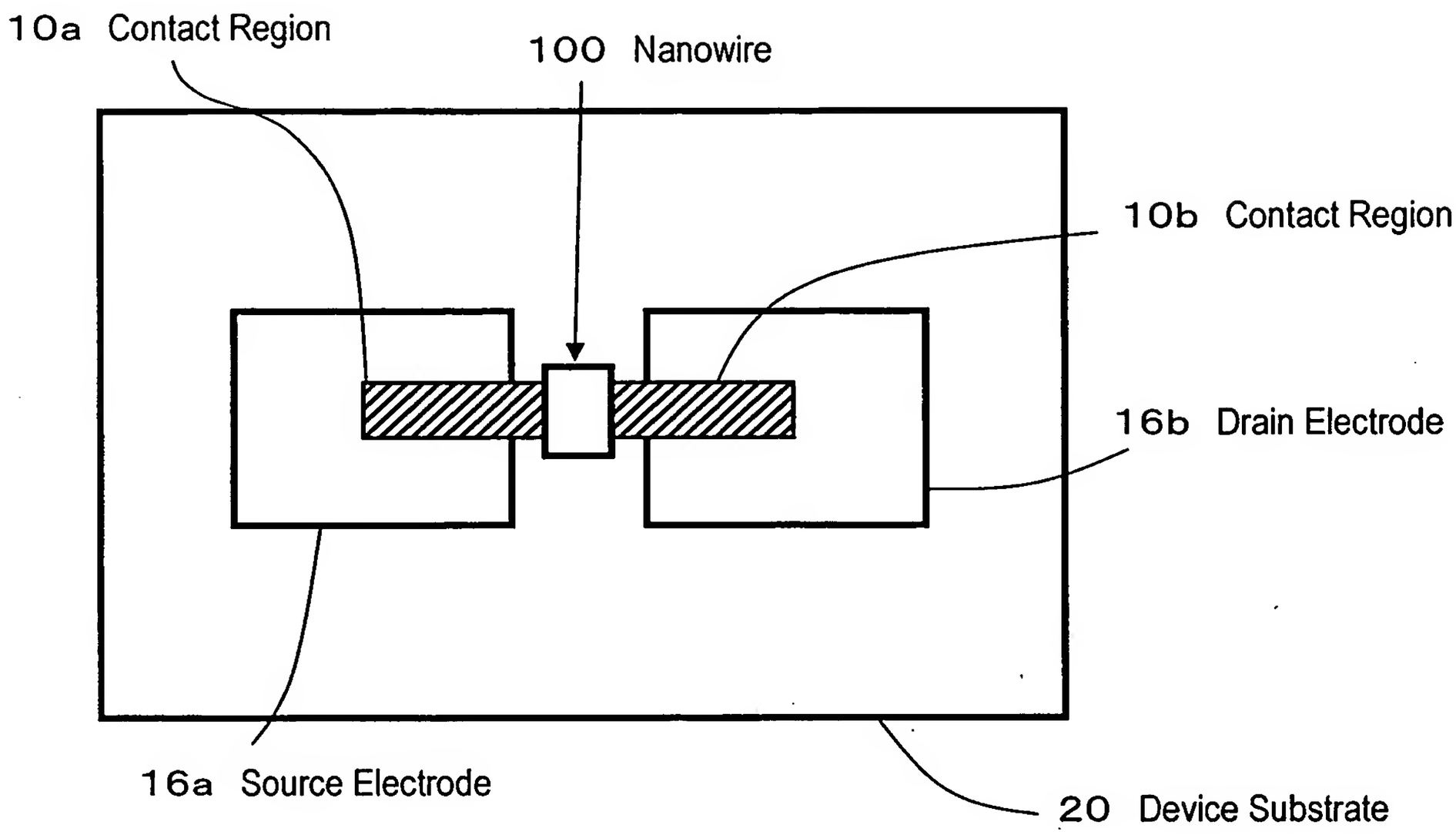

10a Contact Region
100 Nanowire
10b Contact Region
16b Drain Electrode
16a Source Electrode
20 Device Substrate

FIG. 12

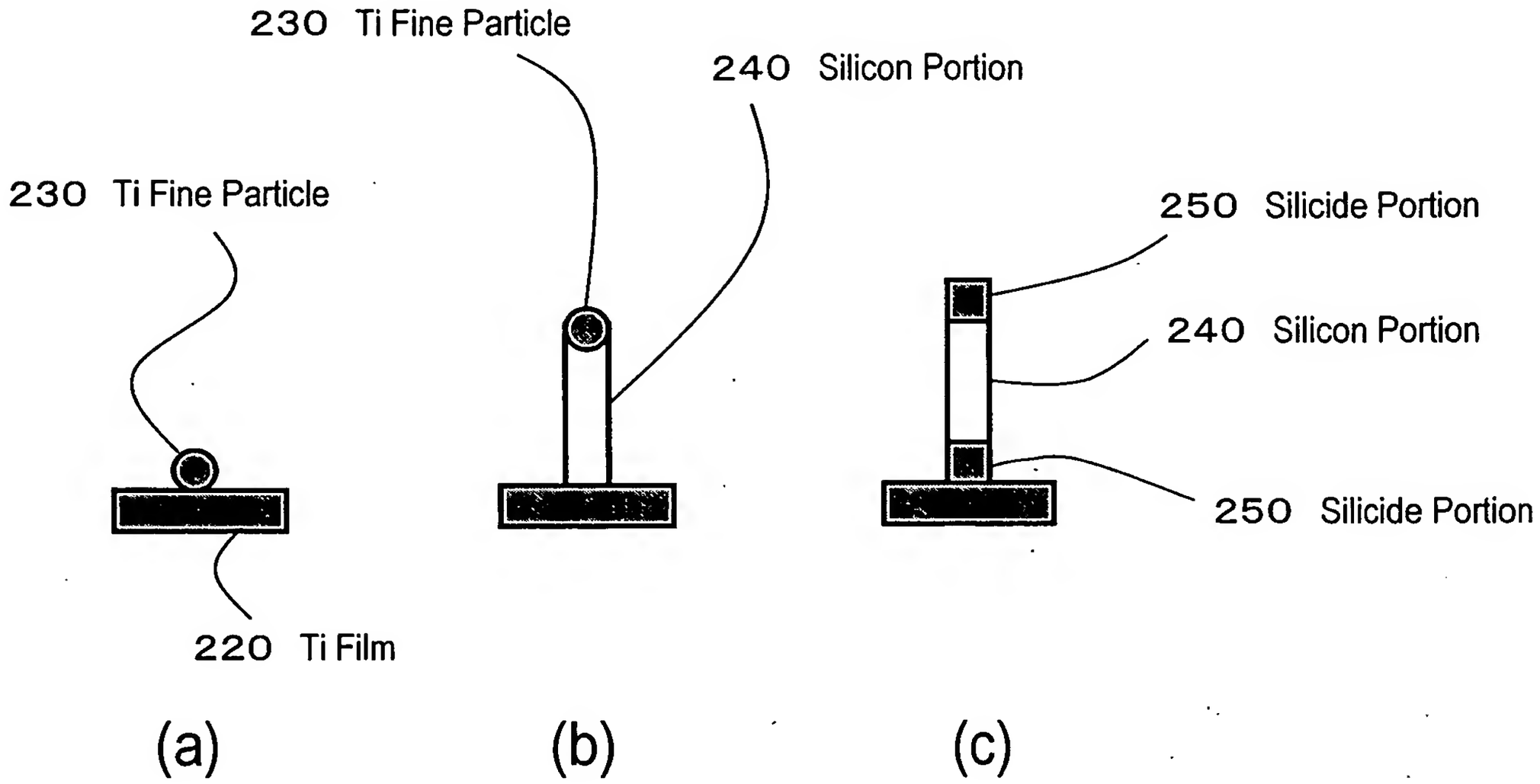
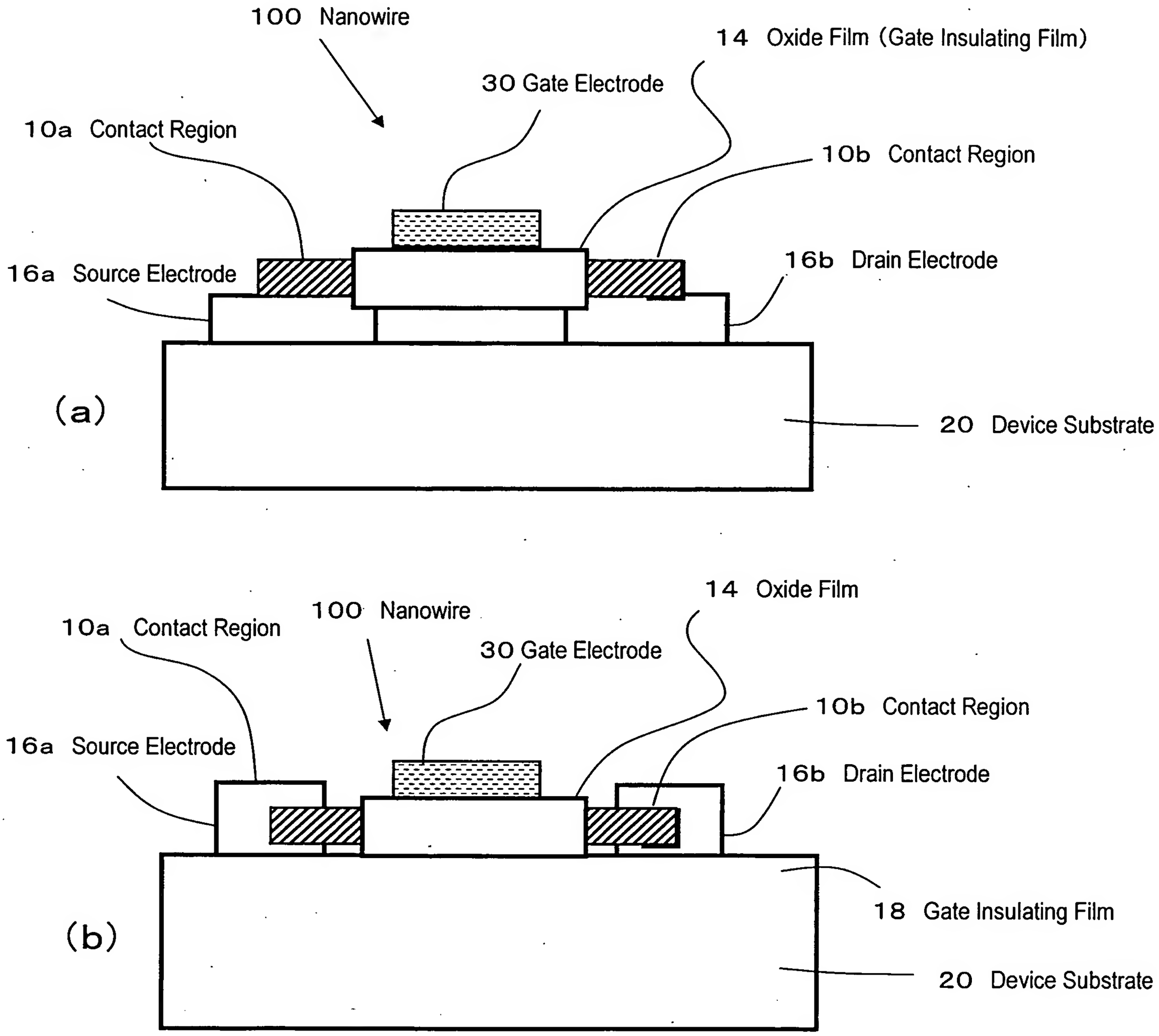

230 Ti Fine Particle
220 Ti Film
(a)
240 Silicon Portion
(b)
250 Silicide Portion
240 Silicon Portion
250 Silicide Portion
(c)

FIG. 13


100 Nanowire
14 Oxide Film (Gate Insulating Film)
30 Gate Electrode
10a Contact Region
10b Contact Region
16a Source Electrode
16b Drain Electrode
(a)
20 Device Substrate
14 Oxide Film
100 Nanowire
10a Contact Region
30 Gate Electrode
10b Contact Region
16a Source Electrode
16b Drain Electrode
18 Gate Insulating Film
(b)
20 Device Substrate